ABSTRACT

A CAM cell with masking made in the form of an integrated circuit, including a first storage cell including a first transistor, first and second inverters in anti-parallel, and a second transistor; a comparison cell, including third and fourth transistors controlling a fifth transistor, connected in series with a sixth inhibiting transistor to a result line; and a second storage cell, including a seventh transistor in series with two inverters in anti-parallel and an eighth transistor, the second storage cell controlling the inhibiting transistor. The first, second, seventh, and eighth transistors may be N-channel transistors, and the third, fourth, fifth, and sixth transistors may be P-channel transistors.